IN THE CLAIMS

Please cancel claims 1-8, 16-17 and 19-20.

Please amend the claims as follows.

1-8 (Cancelled)

9. (Currently amended) An integrated circuit comprising:

a register file bit comprising:

a primary latch having a data input and a data output;

a plurality of secondary latches each having a data input and a data output;

a feedback path from the data ~~output~~ outputs of the plurality of secondary latches to the data input of the ~~first~~ primary latch, the feedback path including a data selection mechanism for selecting any one data output from the plurality of secondary latches to feed back to the data input of the ~~first~~ primary latch; and

a context switch mechanism for switching data between the primary latch and each of the plurality of secondary latches that causes the data on the data output of the primary latch to be written to a selected one of the plurality of secondary latches, and that causes the data on the data output of the selected one secondary latch to be written to the primary latch.

10. (Original) The integrated circuit of claim 9 wherein the context switch mechanism comprises a swap signal coupled to the primary latch.

11. (Original) The integrated circuit of claim 9 wherein the context switch mechanism comprises a delay element between the data output of the primary latch and the data inputs of the plurality of secondary latches.

12. (Original) The integrated circuit of claim 9 wherein the context switch mechanism comprises a delay element in the feedback path.

13. (Original) The integrated circuit of claim 9 wherein the context switch mechanism comprises at least one clock signal that latches data on the data input of the primary latch to the data output of the primary latch and at least one clock signal that latches data on the data input of a secondary latch to the data output of the secondary latch.

14. (Original) The integrated circuit of claim 9 further comprising a plurality of write ports on the data input of the primary latch.

15. (Original) The integrated circuit of claim 9 further comprising a plurality of read ports on the data output of the primary latch.

16-20 (Cancelled)

21. (Currently amended) A method for performing a fast context switch in a register file that includes a primary latch and a plurality of secondary latches that are each selectively connected to the primary latch, the method comprising the steps of:

(A) for each of the plurality of secondary latches, performing the steps of:

(A1) storing a value in the primary latch that corresponds to a selected thread;

(A2) moving the value in the primary latch to a secondary latch;

(B) storing a value in the primary latch that corresponds to an active thread;

(C) selecting one of the secondary latches for performing a context switch with the primary latch; and

(D) performing a context switch between the primary latch and the selected one secondary latch that causes the value in the primary latch to be stored in the selected one secondary latch, and that causes the value in the selected one secondary latch to be stored in the primary latch.

22. (Original) The method of claim 21 wherein the context switch performed in step (D) occurs in a single clock cycle.

STATUS OF THE CLAIMS

Claims 1-22 were originally filed in this patent application. In the pending office action, claim 9 was objected to for an informality and claims 1-17 and 19-22 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,831,623 to Terzian. No claim was allowed. In the first response, claims 1, 8, 16, 19 and 21 were amended and claim 18 was cancelled. In this response, claims 9 and 21 have been amended and claims 1-8, 16-17 and 19-20 have been cancelled. Claims 9-15 and 21-22 are currently pending.